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PATENT APPLICATION

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Patent Application Transmittal Letter

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Sir:

Transmitted herewith for filing under 37 CFR 1.53(b) is a(n): (X) Utility ( ) Design
(X) original patent application,
( ) continuation-in-part application

INVENTOR(S): Que-Won Rhee

TITLE: Configurable Architecture For Virtual Socket Client To An On-Chip Bus Interface Block

Enclosed are:

(X) The Declaration and Power of Attorney. (X) signed ( ) unsigned or partially signed
(X) 6 sheets of drawings (one set) ( ) Associate Power of Attorney
( ) Form PTO-1449 ( ) Information Disclosure Statement and Form PTO-1449
( ) Priority document(s) ( )(Other) _____ (fee $_____)

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INDEPENDENT CLAIMS	3 — 3	0	X $78	$ 0
ANY MULTIPLE DEPENDENT CLAIMS	0		$260	$ 0
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TOTAL FILING FEE				$ 760
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By Nelia T. de Guzman

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Rev 11/99 (TransNew)

- Attach as First Page to Transmitted Papers -

CONFIGURABLE ARCHITECTURE FOR VIRTUAL SOCKET CLIENT TO AN ON-CHIP BUS INTERFACE BLOCK

BACKGROUND

The present invention concerns the interface between two busses and pertains specifically to a configurable architecture for virtual socket client to an on-chip bus interface block.

Within an integrated circuit, it is sometimes necessary to provide an interface between a port of a specialized logic block and an on-chip bus. For example the specialized logic block is proprietary to a particular vendor.

It is difficult and time consuming to design an efficient interface between a port of a specialized logic block and an on-chip bus. Further, any variation in the configuration requirements of the interface can require a complete redesign of the interface.

Modifying a specialized logic block may introduce errors and requires extensive internal knowledge and re-verification time. Efficient block re-use needs flexible glue logic to connect blocks with little or no modifications

SUMMARY OF THE INVENTION

In accordance with the preferred embodiment of the present invention, an interface block provides an interface between an internal bus of an integrated circuit and a socket of a logic block. The interface block includes a synchronization module that performs any needed synchronization between a clock domain of the internal bus and a clock domain of the socket of the logic block. A translation module provides translation of block encoding of the data for data transferred between the

internal bus and the socket of the logic block. A queue module buffers data flowing between the internal bus and the socket of the logic block. A driver module handles low level and electrical drive specifications of the internal bus.

In one embodiment of the present invention, a plurality of buffers is used to pipeline the interface block. For example, a first buffer is located between the synchronization module and the translation module, a second buffer is located between the translation module and the queue module, and a third buffer is located between the queue module and the driver module.

Each of the modules can be individually customized as needed. For example, the synchronization module can be implemented as a null synchronization block where no synchronization is required between clock domains, as a ratio synchronization block where the clock domain of the internal bus is related to the clock domain of the socket of the logic block by a fixed multiplier ratio, or as a full synchronization block where there is no phase relationship between the clock domain of the internal bus and the clock domain of the socket of the logic block.

Customization of interface blocks enables the interface block to be compatible with a variety of different proprietary logic blocks and on-chip busses, as well as to accommodate system design goals. Modularity of the interface block enables rapid assembly while still being tuned for a particular application. These features make this architecture especially suited for rapid, system-on-chip implementations because of the inherent isolation of a specialized logic block and the electrical bus protocol in a rapidly configurable system.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram that illustrates logic blocks within an integrated circuit connected to an on-chip bus where a specialty logic block is connected to the on-chip bus through an interface.

Figure 1, Figure 2, Figure 3, Figure 4 and Figure 5 are block diagrams that illustrate the architecture used for the interface shown in Figure 2 in accordance with various preferred embodiments of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 1 shows an integrated circuit 200 that includes an on-chip bus 15. Attached to on-chip bus 15 are a logic block 201 and a logic block 202. A specialized logic block 10 is connected to on-chip bus 15 through an interface block 19. On-chip bus 15 operates, for example, in accordance with the HP On-chip bus protocol, developed by Hewlett-Packard Company. Alternatively, on-chip bus 15 can operate in accordance with another on-chip bus protocol, such as the Motorola M-bus protocol or the Arm AMBA bus protocol. Specialized logic block 10 is, for example a proprietary logic block that has a socket that requires interface block 19 for compatibility with on-chip bus 15. For example, specialized logic block is a logic block such as a Peripheral Component Interconnect (PCI) interface block, a memory controller, a digital signal processor or an application specific processor. For example, the block protocol used by specialized logic block 10 is a common block interface such as Sand Core Interface, a specific bus protocol

(such as M-Bus protocol, or AMBA client protocol) or a virtual client protocol (such as HP-client interface, or Virtual Client Interface)

Figure 2 shows a configurable architecture for interface block 19. The configurable architecture includes four functional stages. Each functional stage is modular and can be individually configured without grossly affecting neighboring stages.

For example, as shown in Figure 2, a first stage is implemented as a synchronization block 11. Synchronization block 11 synchronizes data between the clock domain of logic block 10 and the clock domain of on-chip bus 15. Synchronization block 11 communicates with specialized logic block 10 utilizing a virtual socket interface protocol via control information on control lines 20 and data on data lines 25.

The second stage of the configurable architecture for interface block 19 is implemented as a translation block 12. Synchronization block 11 and translation block 12 exchange control signals synchronized to the clock domain of on-chip bus 15 via control lines 21 and exchange data signals synchronized to the clock domain of on-chip bus 15 via data lines 26. Translation block 12 converts the block encoding used by the virtual socket interface protocol of specialized logic block 10 to the block encoding used by the protocol implemented on on-chip bus 15. Logic within translation block 12 transforms requests used by the virtual socket interface protocol to equivalent bus requests for the protocol implemented on on-chip bus 15.

The third stage of the configurable architecture for interface block 19 is implemented as a queue block 13. Translation block 12 and queue block 13 exchange control signals via control lines 22 and data signals via data lines

27. Queue block 13 buffers control signals and data signals so that information from both logic block 10 and on-chip bus 15 can flow independently.

The fourth stage of the configurable architecture for interface block 19 is implemented as a driver block 14. Queue block 13 and driver block 14 exchange control signals via control lines 23 and data signals via data lines 28. Driver block 14 generates low-level electrical drive and receive specification of on-chip bus 15. Driver block 14 and on-chip bus 15 exchange control signals via control lines 24 and data signals via data lines 29.

In an alternative embodiment of interface block 19, the stages can be registered to allow pipelined access through interface block 19. This allows operation at higher clock frequencies.

For example, as shown in Figure 3, a first stage is implemented as a synchronization block 31. Synchronization block 31 synchronizes data between the clock domain of logic block 10 and the clock domain of on-chip bus 15. Synchronization block 31 communicates with specialized logic block 10 utilizing a virtual socket interface protocol via control information on control lines 40 and data on data lines 45.

The second stage of the configurable architecture for interface block 19 is implemented as a translation block 32. A clocked buffer 36 receives and transmits control signals from/to synchronization block 11 via control lines 41 and receives and transmits data signals from/to synchronization block 11 via data lines 46. Clocked buffer 36 receives and transmits control signals from/to translation block 12 via control lines 51 and receives and transmits data signals from/to translation block 12 via data lines 46. Translation block

32 converts the block encoding used by the virtual socket interface protocol of specialized logic block 10 to the block encoding used by the protocol implemented on on-chip bus 15. Logic within translation block 32 transforms requests used by the virtual socket interface protocol to equivalent bus requests for the protocol implemented on on-chip bus 15.

The third stage of the configurable architecture for interface block 19 is implemented as a queue block 33. A clocked buffer 37 receives and transmits control signals from/to translation block 12 via control lines 42 and receives and transmits data signals from/to translation block 12 via data lines 47. Clocked buffer 37 receives and transmits control signals from/to queue block 33 via control lines 52 and receives and transmits data signals from/to queue block 33 via data lines 57. Queue block 33 buffers control signals and data signals so that information from both logic block 10 and on-chip bus 15 can flow independently.

The fourth stage of the configurable architecture for interface block 19 is implemented as a driver block 34. A clocked buffer 38 receives and transmits control signals from/to queue block 33 via control lines 43 and receives and transmits data signals from/to queue block 13 via data lines 48. Clocked buffer 38 receives and transmits control signals from/to driver block 34 via control lines 53 and receives and transmits data signals from/to driver block 34 via data lines 58. Driver block 34 generates low-level electrical drive and receive specification of on-chip bus 15. Driver block 34 and on-chip bus 15 exchange control signals via control lines 44 and data signals via data lines 49.

Also, in the preferred embodiments of the present invention, different stages can be swapped out depending upon the functionality required for interface block 19. For example, Figure 4 shows the embodiment shown in Figure 1, however, synchronization block 11 has been implemented as a null synchronization block 61. Null synchronization block 61 is used when no synchronization is needed between the clock domain of logic block 10 and the clock domain of on-chip bus 15.

If the clock domain of logic block 10 is related to the clock domain of on-chip bus 15 by a fixed multiplier ratio, null synchronization block 61 can be replaced by a ratio synchronization block 81, as shown in Figure 5. No other changes to interface block 19 are necessary.

If the clock domain of logic block 10 is not phase related to the clock domain of on-chip bus 15, null synchronization block 61 or ratio synchronization block 81, can be replaced by a full synchronization block 101, as shown in Figure 6. No other changes to interface block 19 are necessary.

The foregoing discussion discloses and describes merely exemplary methods and embodiments of the present invention. As will be understood by those familiar with the art, the invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. Accordingly, the disclosure of the present invention is intended to be illustrative, but not limiting, of the scope of the invention, which is set forth in the following claims.

CLAIMS

I Claim:

1. On an integrated circuit, an interface block that provides an interface between an internal bus of the integrated circuit and a socket of a logic block, the interface block comprising:

a synchronization module that performs any needed synchronization between a clock domain of the internal bus and a clock domain of the socket of the logic block;

a translation module that, for data transferred between the internal bus and the socket of the logic block, provides translation of block encoding of the data;

a queue module, that buffers data flowing between the internal bus and the socket of the logic block; and,

a driver module that handles low level and electrical drive specifications of the internal bus.

2. An interface block as in claim 1 wherein the synchronization module can be implemented as one of:

a null synchronization block where no synchronization is required between the clock domain of the internal bus and the clock domain of the socket of the logic block;

a ratio synchronization block where the clock domain of the internal bus is related to the clock domain of the socket of the logic block by a fixed multiplier ratio; and,

a full synchronization block where there is no phase relationship between the clock domain of the internal bus and the clock domain of the socket of the logic block.

3. An interface block as in claim 1 additionally comprising a plurality of buffers used to pipeline the interface block, the plurality of buffers including:

a first buffer between the synchronization module and the translation module;

a second buffer between the translation module and the queue module; and,

a third buffer between the queue module and the driver module.

4. A method for providing an interface between an internal bus of an integrated circuit and a socket of a logic block within the integrated circuit, the method comprising the steps of:

(a) performing any needed synchronization between a clock domain of the internal bus and a clock domain of the socket of the logic block within a synchronization module;

(b) providing any required translation of block encoding of data transferred between the internal bus and the socket of the logic block using a translation module;

(c) buffering data flowing between the internal bus and the socket of the logic block using a queue module; and,

(d) handling low level and electrical drive specifications of the internal bus using a driver module.

5. A method as in claim 4 wherein step (a) comprises the following substeps:

(a.1) using a null synchronization block where no synchronization is required between the clock domain of the internal bus and the clock domain of the socket of the logic block;

(a.2) using a ratio synchronization block where the clock domain of the internal bus is related to the clock domain of the socket of the logic block by a fixed multiplier ratio; and,

(a.3) using a full synchronization block where there is no phase relationship between the clock domain of the internal bus and the clock domain of the socket of the logic block.

6. A method as in claim 4 additionally comprising the following step:

(e) providing buffers between modules to allow pipelined operation.

7. On an integrated circuit, an interface block that provides an interface between an internal bus of the integrated circuit and a socket of a logic block, the interface block comprising:

a plurality of modules connected in series, where any needed synchronization between a clock domain of the internal bus and a clock domain of the socket of the logic block, any required translation of block encoding of data, any buffering of data flowing between the internal bus and

the socket of the logic block, and any low level and electrical drive specifications of the internal bus are performed by the plurality of modules so that one module from the plurality of modules performs a single function.

8. An interface block as in claim 7 wherein a first module in the plurality of modules is a synchronization module that performs any needed synchronization between the clock domain of the internal bus and the clock domain of the socket of the logic block.

9. An interface block as in claim 7 wherein one module in the plurality of modules is a translation module that, for the data transferred between the internal bus and the socket of the logic block, provides translation of block encoding of the data.

10. An interface block as in claim 7 wherein one module in the plurality of modules is a queue module, that buffers the data flowing between the internal bus and the socket of the logic block.

11. An interface block as in claim 7 wherein one module in the plurality of modules is a driver module that handles low level and electrical drive specifications of the internal bus.

12. An interface block as in claim 7 additionally comprising a plurality of buffers situated between modules in the plurality of modules, the buffers used to pipeline the interface block.

ABSTRACT

An interface block provides an interface between an internal bus of an integrated circuit and a socket of a logic block. The interface block includes a synchronization module that performs any needed synchronization between a clock domain of the internal bus and a clock domain of the socket of the logic block. A translation module provides translation of block encoding of the data for data transferred between the internal bus and the socket of the logic block. A queue module buffers data flowing between the internal bus and the socket of the logic block. A driver module handles low level and electrical drive specifications of the internal bus.

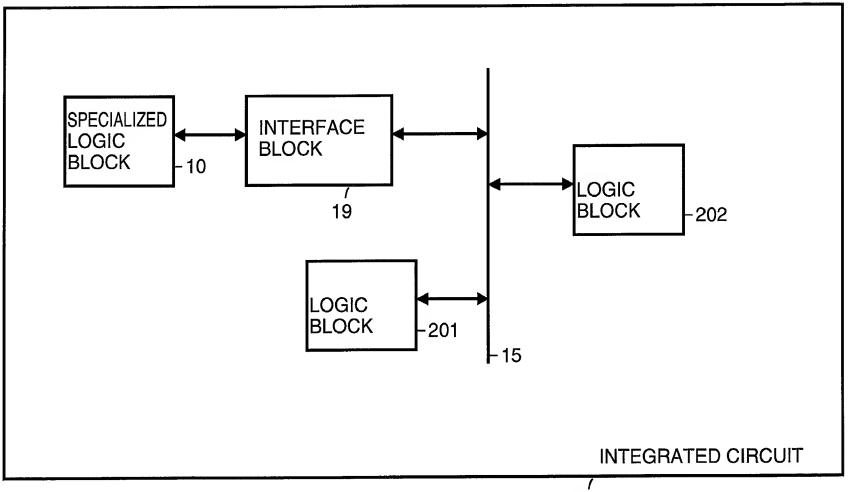
SPECIALIZED LOGIC BLOCK
10
INTERFACE BLOCK
19
LOGIC BLOCK
202
LOGIC BLOCK
201
15
INTEGRATED CIRCUIT
200

FIGURE 1

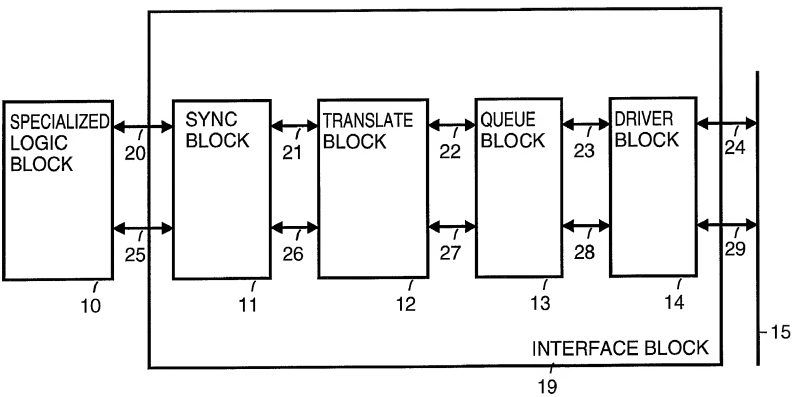
SPECIALIZED LOGIC BLOCK
SYNC BLOCK
TRANSLATE BLOCK
QUEUE BLOCK
DRIVER BLOCK
INTERFACE BLOCK
10
11
12
13
14
15
19
20
21
22
23
24
25
26
27
28
29

FIGURE 2

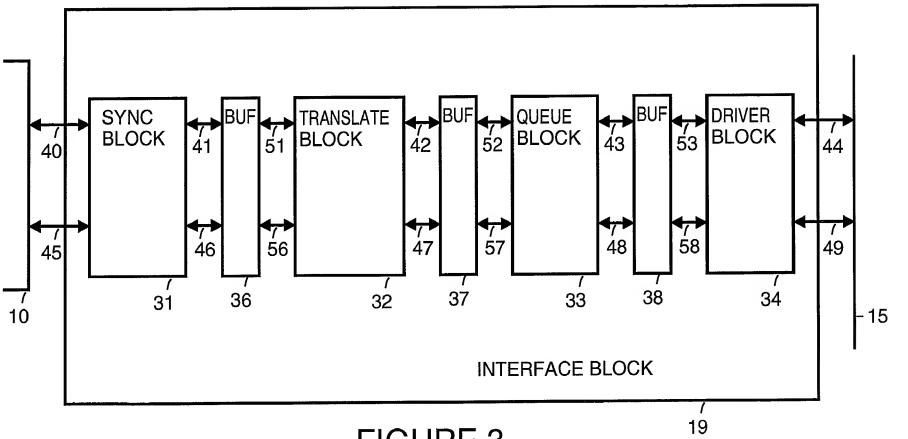
SYNC BLOCK
BUF
TRANSLATE BLOCK
BUF
QUEUE BLOCK
BUF
DRIVER BLOCK
40
41
51
42
52
43
53
44
45
46
56
47
57
48
58
49
10
31
36
32
37
33
38
34
15
INTERFACE BLOCK
19

FIGURE 3

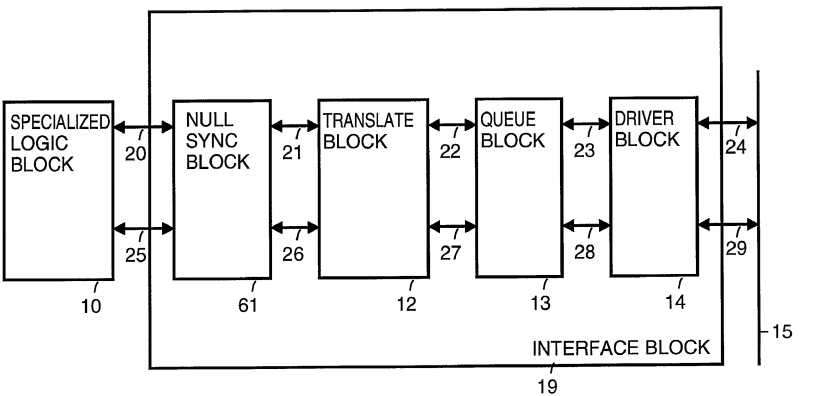
SPECIALIZED LOGIC BLOCK
NULL SYNC BLOCK
TRANSLATE BLOCK
QUEUE BLOCK
DRIVER BLOCK
INTERFACE BLOCK
20
21
22
23
24
25
26
27
28
29
10
61
12
13
14
15
19

FIGURE 4

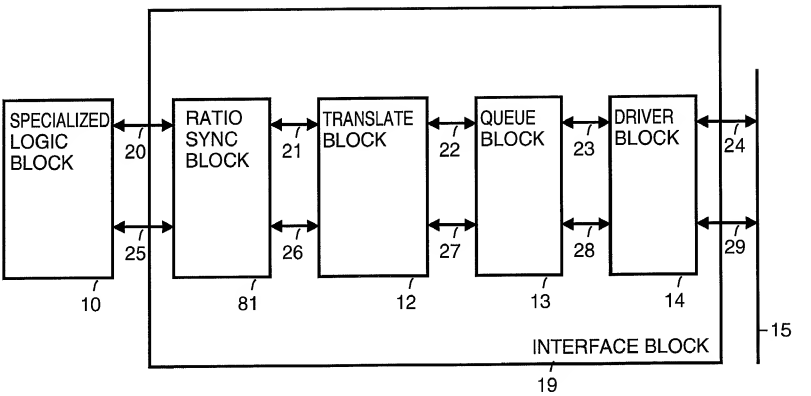
SPECIALIZED LOGIC BLOCK
RATIO SYNC BLOCK
TRANSLATE BLOCK
QUEUE BLOCK
DRIVER BLOCK
INTERFACE BLOCK
10
81
12
13
14
15
19
20
21
22
23
24
25
26
27
28
29

FIGURE 5

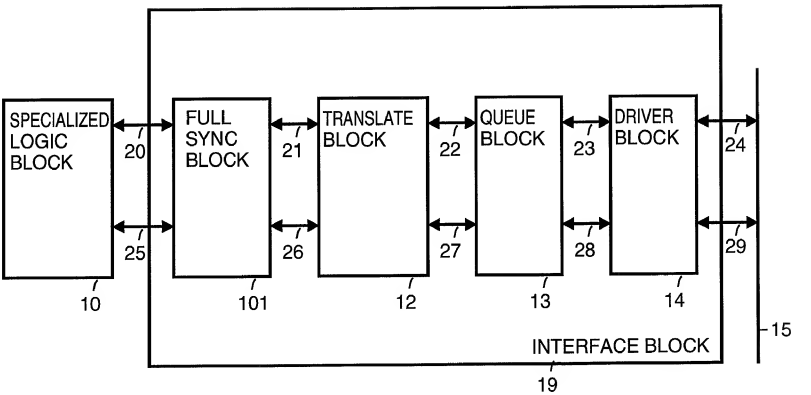

FIGURE 6

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO. 10991663-1

As a below named inventor, I hereby declare that:

My residence/post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Configurable Architecture For Virtual Socket Client To An On-Chip Bus Interface Block

the specification of which is attached hereto unless the following box is checked:

( ) was filed on _____ as US Application Serial No. or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56.

Foreign Application(s) and/or Claim of Foreign Priority

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE FILED	PRIORITY CLAIMED UNDER 35 U S.C. 119
			YES: ___ NO. ___
			YES: ___ NO. ___

Provisional Application

I hereby claim the benefit under Title 35, United States Code Section 119(e) of any United States provisional application(s) listed below:

APPLICATION SERIAL NUMBER	FILING DATE

U. S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (patented/pending/abandoned)

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

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Brian R. Short

(650) 857-6021

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Inventor: Que-Won Rhee **Citizenship:** US

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Post Office Address: Same as residence

Won Rhee

Inventor's Signature

11/2/99

Date